

REMARKS

Favorable reconsideration of this application, in light of the above amendments and following remarks, is respectfully requested.

Claims 1-2 and 4-13 are currently pending, with Claims 2, 4, 6, 9-11 and 13 being withdrawn as directed to non-elected inventions. Claims 1 and 8 have been amended; and Claim 3 has been canceled without prejudice by the present amendment. No new matter has been added.

In the outstanding Office Action, the drawings were objected to under 37 C.F.R. § 1.83(a) as failing to show every feature recited in the claims; Claims 1, 5, 8 and 12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,777,659 to Schwarte (hereinafter “the ‘659 patent”) in view of U.S. Patent No. 4,165,471 to Ahrenkeil (hereinafter “the ‘471 patent”); Claim 3 was rejected under 35 U.S.C. § 103(a) as being unpatentable over the ‘659 patent and the ‘471 patent, further in view of U.S. Patent No. 4,136,292 to Suzuki et al. (hereinafter “the ‘292 patent”); and Claim 7 was rejected under 35 U.S.C. § 103(a) as being unpatentable over the ‘659 patent and the ‘471 patent, further in view of U.S. Patent No. 6,548,352 to Rhodes (hereinafter “the ‘352 patent”).

Regarding the objection to Fig. 1 under 37 CFR 1.83(a), Claim 8 has been amended to clarify that both a p-type well and an n-type well are not formed in the photodetector layer. The objection to the drawing is believed to have been overcome, thus rendering the objection moot in light of the amendment.

Claim 1 has been amended to recite:

A time-of-flight range-finding sensor for range-finding by reading a signal, which depends on a delay time of repetitive light pulses transmitted from a light source and then reflected by a target object to be measured, the time-of-flight range-finding sensor comprising:

a p-type semiconductor substrate having a p-type photodetector layer and a p-type well formed at a surface of the semiconductor substrate so as to encircle the photodetector layer in a plan view, the p-type well having higher concentration than the semiconductor substrate;

an insulator layer formed on the photodetector layer;
two conductive photo-gate electrodes provided on the insulator layer above the photodetector layer, adjacently disposed so as to define a gap between the two photo-gate electrodes, and being transparent for a wavelength of a light reflected by the target object; and

two MOS transistors formed in the p-type well so as to sandwich the photo-gate electrodes, each of the MOS transistors having an n-type floating diffusion layer serving as a source region, which is disposed at a boundary between the photodetector layer and the p-type well, configured to extract charges from the photodetector layer,

wherein a uniform optical path exists along the full-width of the gap, and regions of the semiconductor substrate beneath the two photo-gate electrodes and beneath the gap are used as a photodetector layer.

The changes to Claim 1 are supported by Fig. 1 of the specification showing, in part, a p-type well encircling a photodetector layer, and Claim 3, as well as other features shown in Fig. 7 and described in the specification, page 15.

In the rejection of Claim 1 under 35 U.S.C. §103(a), the Office Action relied on the '471 patent to overcome the deficiencies of the '659 patent. The '292 patent was cited in regards to the features of Claim 3 not taught in the combination of the '659 and the '471 patents. As the features of Claim 3 have now been included in Claim 1, all three of the above cited references are discussed herein with respect to Claim 1.

The '659 patent describes an apparatus for detecting phase and amplitude of electromagnetic waves with modulation photogates and accumulation gates arranged in parallel in narrow long strips and wherein the accumulation gates are in the form of reading-out diodes. However, Applicants respectfully submit that the '659 patent does not disclose a p-type semiconductor substrate having a p-type photodetector layer and a p-type well formed at a surface of the semiconductor substrate so as to encircle the photodetector layer in a plan view, the p-type well having higher concentration than the semiconductor substrate, as recited in amended Claim 1.

Fig. 3 of the '659 patent shows two accumulation gates 4 and 5 implemented by pn-junction diodes sandwich modulation photogates 1 and 2, and anode terminal of the pn-

junction diode is provided at the bottom of substrate. In accordance with the photomixing detector (PMD) described in the '659 patent, in the possible voltage reading-out mode, the photocharges, which are distributed in accordance with the push-pull modulation voltages, are stored on the capacitances of the accumulation gates 4, 5, on the barrier layer capacitances of the reading-out diodes, which are connected in the blocking direction of the pn-junction diodes. See the '659 patent, column 4, lines 15-22. Further, FIG. 11 of the '659 patent shows a PMD-pixel 10 implemented by two reading-out diodes.

Thus, Applicants respectfully submit that the '659 patent also fails to show two MOS transistors formed in the p-type well so as to sandwich the photo-gate electrodes, each of the MOS transistors having an n-type floating diffusion layer serving as a source region, which is disposed at a boundary between the photodetector layer and the p-type well and configured to extract charges from the photodetector layer, as recited in amended Claim 1.

The '471 patent is directed to a light sensing apparatus which employs a GaAsP MOS light receiving element to which a potential is applied for creating a depletion region. The Office Action appears to have admitted that the '471 patent fails to disclose a teaching of first MOS transistors with their gates coupled to diffusion layers because the '292 patent is cited for providing this feature. Applicant respectfully submits that the '471 patent also does not teach two MOS transistors formed in the p-type well so as to sandwich the photo-gate electrodes, each of the MOS transistors having an n-type floating diffusion layer serving as a source region, which is disposed at a boundary between the photodetector layer and the p-type well and configured to extract charges from the photodetector layer, as recited in amended Claim 1.

Further, Applicant respectfully submits that the '471 patent does not disclose a p-type semiconductor substrate having a p-type photodetector layer and a p-type well formed at a surface of the semiconductor substrate so as to encircle the photodetector layer in a plan

view, the p-type well having higher concentration than the semiconductor substrate, as recited in amended Claim 1.

The '292 patent is directed to a voltage sensing circuit of differential input type including at least on differential amplifier circuit connected between two complementary data lines of a semiconductor memory. To overcome deficiencies in the combination of the '659 patent and the '471 patent, the '292 patent was relied on for "two data lines ready to be coupled to any two sources of data signals coupled to two MOS transistors". However, the MOS transistors of the '292 patent are not formed in a p-type well so as to sandwich photogate electrodes. Thus, Applicants respectfully submit that the '292 patent fails to disclose two MOS transistors formed in the p-type well so as to sandwich the photo-gate electrodes, each of the MOS transistors having an n-type floating diffusion layer serving as a source region, which is disposed at a boundary between the photodetector layer and the p-type well and configured to extract charges from the photodetector layer, as recited in amended Claim 1.

Further, Applicant respectfully submits that the '292 patent does not disclose a p-type semiconductor substrate having a p-type photodetector layer and a p-type well formed at a surface of the semiconductor substrate so as to encircle the photodetector layer in a plan view, the p-type well having higher concentration than the semiconductor substrate, as recited in amended Claim 1.

Consequently, no matter how the teachings of the '659 patent, the '471 patent and the '292 patent are combined, the combination fails to teach or suggest a p-type semiconductor substrate having a p-type photodetector layer and a p-type well formed at a surface of the semiconductor substrate so as to encircle the photodetector layer in a plan view, and two MOS transistors formed in the p-type well so as to sandwich the photo-gate electrodes, as recited in amended Claim 1.

Thus, Applicants respectfully submit that the rejection of Claim 1 (and all associated dependent claims) is rendered moot by the present amendment to Claim 1.

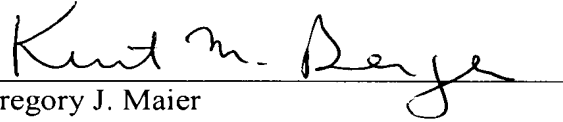
In regard to dependent Claim 7, the Office Action cites the '352 patent, in view of the '659 patent and the '471 patent, as teaching photogate electrodes made of polysilicon. The '352 patent describes a multi-layered gate for use in a CMOS or CCD imager formed with a second gate at least partially overlapping it. However, the addition of the '352 patent does not overcome the deficiencies of the '659 patent and the '471 with respect to a p-type semiconductor substrate having a p-type photodetector layer and a p-type well formed at a surface of the semiconductor substrate so as to encircle the photodetector layer in a plan view, the p-type well having higher concentration than the semiconductor substrate or two MOS transistors formed in the p-type well so as to sandwich the photo-gate electrodes, each of the MOS transistors having an n-type floating diffusion layer serving as a source region, which is disposed at a boundary between the photodetector layer and the p-type well and configured to extract charges from the photodetector layer, as recited in amended Claim 1.

Thus, Applicants respectfully submit that the rejection of Claim 7 is rendered moot by the present amendment to Claim 1.

Accordingly, the outstanding rejections are traversed and the pending claims are believed to be in condition for formal allowance. An early and favorable action to that effect is, therefore, respectfully requested.

Respectfully submitted,

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A handwritten signature in black ink, reading "Kurt M. Berger", is written over a horizontal line.

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